10 Audio Interfaces

10.1 Audio Interface

The audio interface circuit consists of:

- Stereo audio CODEC
- Dual audio inputs and outputs
- A configurable PCM, I^2S or SPDIF interface

Figure 10.1 shows the functional blocks of the interface. The CODEC supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the CODEC each contain two independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

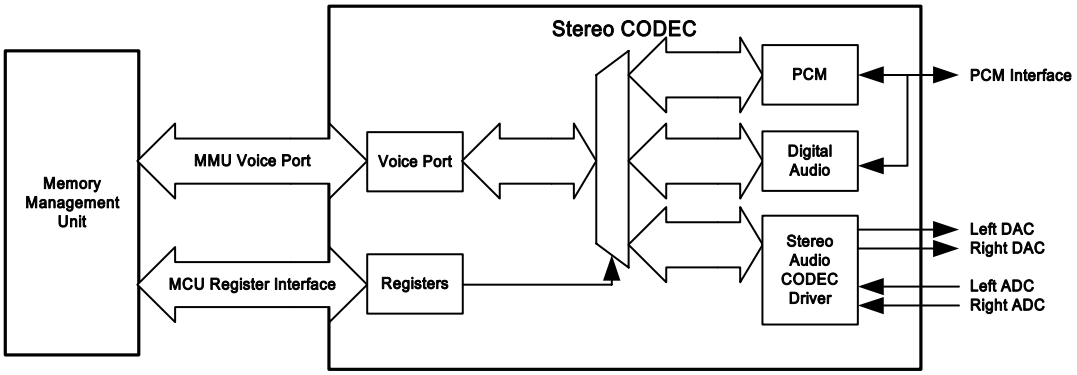


Figure 10.1: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM CODEC interface described in Section 10.3 which means each of the audio buses are mutually exclusive in their usage. Table 10.1 lists these alternative functions.

PCM Interface	SPDIF Interface	I^2S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC	-	WS
PCM_CLK	-	SCK

Table 10.1: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

10.1.1 Audio Input and Output

The audio input circuitry consists of a dual audio input that can be configured to be either single-ended or fully differential and programmed for either microphone or line input. It has an analogue and digital programmable gain stage for optimisation of different microphones.

The audio output circuitry consists of a dual differential class A-B output stage.

10.2 Stereo Audio CODEC Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I^2S
- Support for IEC-60958 standard stereo digital audio bus standards, e.g. S/PDIF and AES3/EBU
- Support for PCM interfaces including PCM master CODECs that require an external system clock

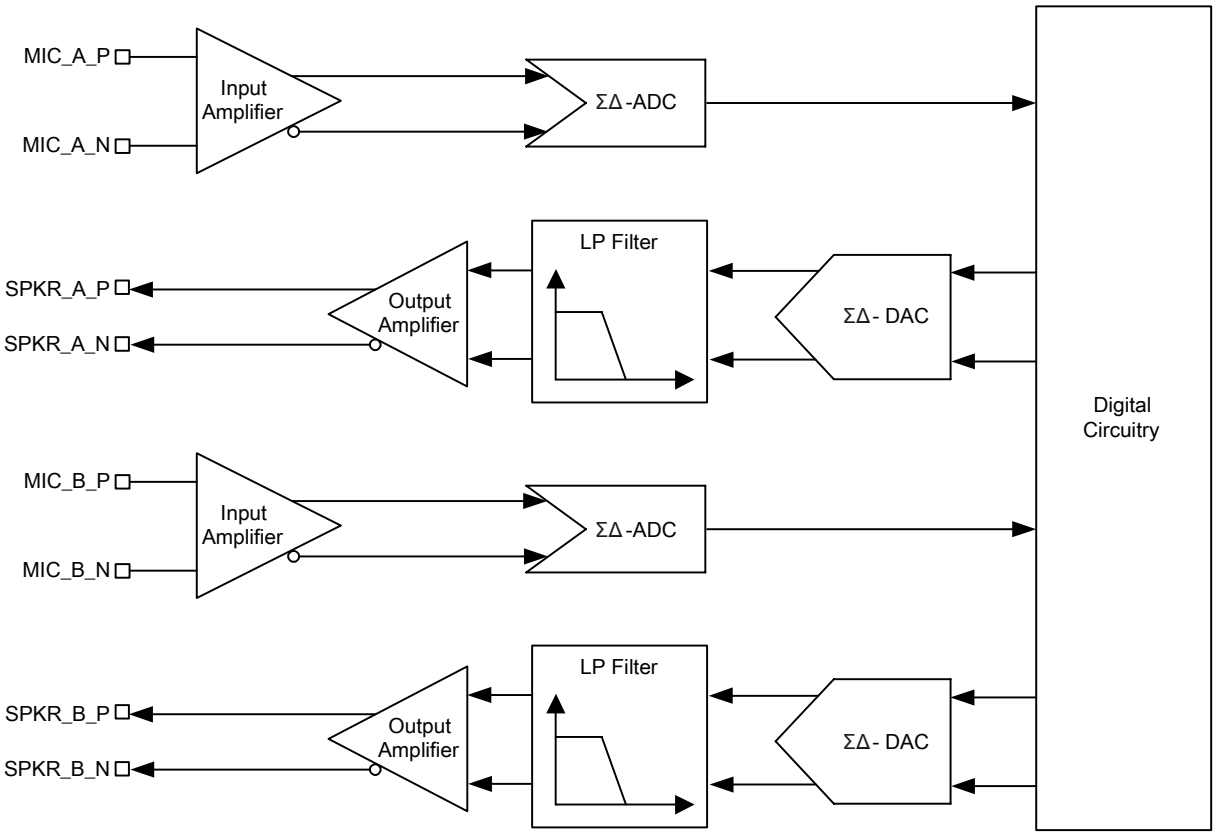


Figure 10.2: Stereo Codec Audio Input and Output Stages

The stereo audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components.

Important Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio input and output. With respect to software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel for both input and output.

For mono operation this data sheet uses the left channel for standard mono operation for audio input and output and with respect to software and any registers, channel 0 or channel A represents the standard mono channel for audio input and output. In mono operation the second channel which is the right channel, channel 1 or channel B could be used as a second mono channel if required and this channel is referred to as the auxilliary mono channel for audio input and output.

10.2.1 Stereo CODEC Set-up

The configuration and control of the ADC is through VM functions which are described in appropriate BlueLab Multimedia documentation. This section is an overview of the parameters that can be set up using the VM functions.

The Kalimba DSP can communicate its requirements of the CODEC to the MCU, and therefore also to the VM, by exchange of messages. The messages used between the Kalimba DSP and the embedded MCU are based on interrupts:

- 1 interrupt between the MCU and Kalimba DSP
- 1 interrupt between the Kalimba DSP and the MCU

Message content is transmitted using shared memory. There are VM and DSP library functions to send and receive messages; refer to BlueLab Multimedia documentation for further details.

10.2.2 ADC

The ADC consists of two second-order Sigma Delta converters allowing two separate channels that are identical in functionality, as shown in Figure 10.2.

10.2.3 ADC Sample Rate Selection

Each ADC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.05kHz
- 24kHz
- 32kHz
- 44.1kHz

10.2.4 ADC Gain

The ADC contains two gain stages for each channel, an analogue and a digital gain stage.

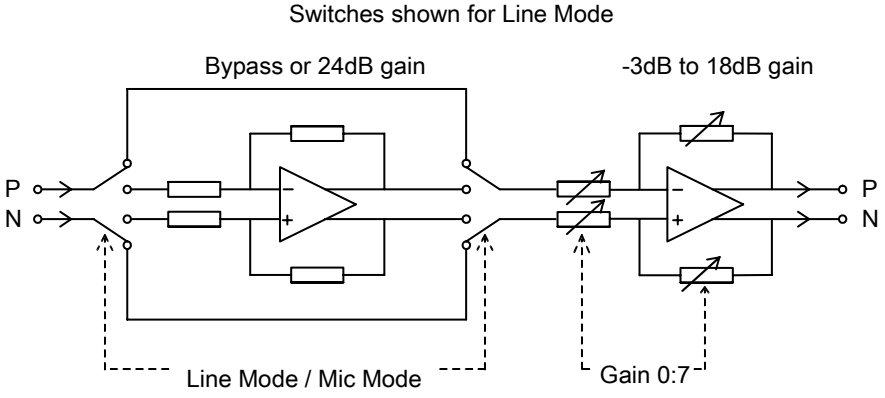
The digital gain stage has a programmable selection value in the range of 0 to 15 with the associated ADC gain settings summarised in Table 10.2. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Contact CSR for more information.

Gain Selection Value	ADC Digital Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5

Gain Selection Value	ADC Digital Gain Setting (dB)
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

Table 10.2: ADC Digital Gain Rate Selection

The ADC analogue amplifier is a two-stage amplifier. The first stage of the analogue amplifier is responsible for selecting the correct gain for either microphone input or line input and therefore has two gain settings, one for the microphone and one for the line input. See Section 10.2.9 and Section 10.2.10 for details on the microphone and line inputs, respectively. The first stage amplifier has a selectable 24dB gain stage for the microphone and this creates the dual programmable gain required for the microphone or the line input. The equivalent block diagram for the two stage is shown in Figure 10.3.



Microphone Mode input impedance = 6kΩ

Line mode input impedance = 6kΩ to 30kΩ

Figure 10.3: ADC Analogue Amplifier Block Diagram

The second stage of the analogue amplifier shown in Figure 10.3 has a programmable gain with seven individual 3dB steps. By combining the 24dB gain selection of the microphone input with the seven individual 3dB gain steps, the overall range of the analogue amplifier is approximately -3dB to 42dB in 3dB steps. The overall gain control of the ADC is controlled by the a VM function.

10.2.5 DAC

The DAC consists of two third-order Sigma Delta converters allowing two separate channels that are identical in functionality as shown in Figure 10.2.

10.2.6 DAC Sample Rate Selection

Each DAC supports the following samples rates:

- 8kHz
- 11.025kHz
- 12kHz
- 16kHz
- 22.050kHz
- 24kHz

- 32kHz
- 44.1kHz
- 48kHz

10.2.7 DAC Gain

The DAC contains two gain stages for each channel: a digital and an analogue gain stage.

The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings. This is summarised in Table 10.3. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Contact CSR for more information.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

Table 10.3: DAC Digital Gain Rate Selection

The overall gain control of the DAC is controlled by a VM function. This setting is a combined function of the digital and analogue amplifier settings, therefore, for a 1V rms nominal digital output signal from the digital gain stage of the DAC, the following approximate output values of the analogue amplifier of the DAC can be expected:

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	3
6	0
5	-3
4	-6
3	-9
2	-12
1	-15
0	-18

Table 10.4: DAC Analogue Gain Rate Selection

10.2.8 IEC 60958 Interface

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and allows the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the two industry standards:

- AES/EBU
- Sony and Philips interface specification SPDIF

The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4.

The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins. The input and output stages of the SPDIF pins can interface to:

- A 75Ω coaxial cable with an RCA connector, see Figure 10.4
- An optical link that uses Toslink optical components, see Figure 10.5.

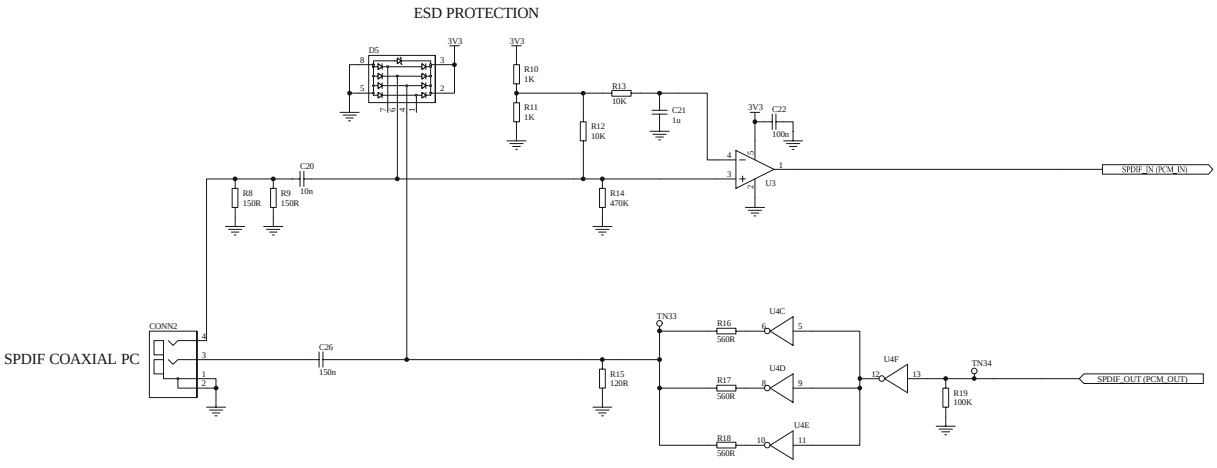


Figure 10.4: Example Circuit for SPDIF Interface (Co-Axial)

Figure 10.5: Example Circuit for SPDIF Interface (Optical)

10.2.9 Microphone Input

The audio input is intended for use from 1µA@94dB SPL to about 10µA@94dB SPL. With biasing resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40dBV and –60dBV. The microphone for each channel should be biased as shown in Figure 10.6. The microphone bias, MIC_BIAS, derives its power from the BAT_P and also requires a 1µF capacitor on its output.

The MIC_BIAS is like any voltage regulator and requires a minimum load to maintain regulation. The MIC_BIAS maintains regulation within the limits 0.199 - 1.229mA. This means, if a microphone is used that sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.

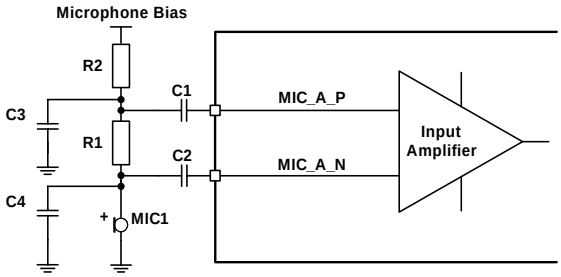


Figure 10.6: Microphone Biasing (Single Channel Shown)

The input impedance at AUDIO_IN_N_LEFT, AUDIO_IN_P_LEFT, AUDIO_IN_N_RIGHT and AUDIO_IN_P_RIGHT is typically 6.0kΩ. C1 and C2 should be 150nF if bass roll-off is required to limit wind noise on the microphone. R1 sets the microphone load impedance and is normally in a range of 1 - 2kΩ. R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Values should be selected as required. R2 may be connected to a convenient supply, in which case the bias network is permanently enabled, or to the MIC_BIAS output (which is ground referenced and provides good rejection of the supply), which may be configured to provide bias only when the microphone is required.

The microphone bias provides a 4-bit programmable output voltage, shown in Table 10.5, with a 4-bit programmable output current, shown in Table 10.6.

The basic specifications of the microphone bias include:

- Power supply, BAT_P: the minimum input battery voltage should be “Output voltage” + “Drop-out voltage”, and the maximum input voltage is 4.9V. VDD_AUDIO - 1.5V typical.
- Drop-out voltage: 300mV (minimum) guaranteed for all voltage/current output setup
- Output voltage: 4-bit programmable between 1.8 - 3.6V, tolerance 90 - 110%
- Output current: 200uA – 1.229mA, maximum current guaranteed to be >1mA
- Load capacitance: unconditionally stable for 1uF ±20% and 2.2uF ±20% pure C

Output Step	VOL_SET[3:0]	Min	Typ	Max	Units
0	0000	-	1.71	-	V
1	0001	-	1.76	-	V
2	0010	-	1.82	-	V
3	0011	-	1.87	-	V
4	0100	-	1.95	-	V
5	0101	-	2.02	-	V
6	0110	-	2.10	-	V
7	0111	-	2.18	-	V
8	1000	-	2.32	-	V
9	1001	-	2.43	-	V
10	1010	-	2.56	-	V
11	1011	-	2.69	-	V
12	1100	-	2.90	-	V
13	1101	-	3.08	-	V
14	1110	-	3.33	-	V
15	1111	-	3.57	-	V

Table 10.5: Voltage Output Steps

Output Step	CUR_SET[3:0]	Min	Typ	Max	Units
0	0000	-	0.199	-	mA
1	0001	-	0.284	-	mA
2	0010	-	0.336	-	mA
3	0011	-	0.419	-	mA
4	0100	-	0.478	-	mA
5	0101	-	0.529	-	mA
6	0110	-	0.613	-	mA
7	0111	-	0.672	-	mA
8	1000	-	0.754	-	mA

Output Step	CUR_SET[3:0]	Min	Typ	Max	Units
9	1001	-	0.809	-	mA
10	1010	-	0.862	-	mA
11	1011	-	0.948	-	mA
12	1100	-	1.004	-	mA
13	1101	-	1.091	-	mA
14	1110	-	1.142	-	mA
15	1111	-	1.229	-	mA

Table 10.6: Current Output Steps

Note:

For BAT_P, the PSRR @ 100Hz - 22kHz, with >300mV supply headroom, decoupling capacitor of 1.1µF, is typically 58.9dB and worst case 53.4dB.

For VDD_AUDIO, the PSRR @ 100Hz - 22kHz, decoupling capacitor of 1.1µF, is typically 88dB and worst case 60dB.

10.2.10 Line Input

If the input analogue gain is set to less than 24dB, BlueCore5-Multimedia External automatically selects line input mode. In line input mode the first stage of the amplifier is automatically disabled, providing additional power saving. In line input mode the input impedance varies from 6kΩ - 30kΩ, depending on the volume setting. Figure 10.7 and Figure 10.8 show two circuits for line input operation and show connections for either differential or single-ended inputs.

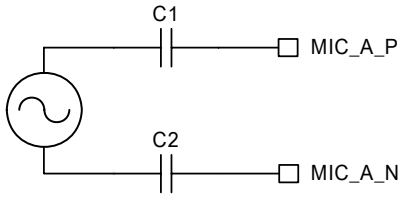


Figure 10.7: Differential Input (Single Channel Shown)

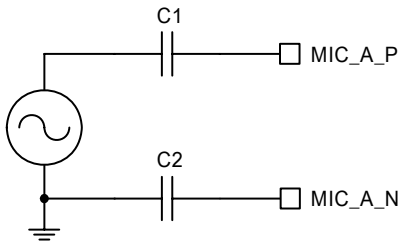


Figure 10.8: Single-Ended Input (Single Channel Shown)

10.2.11 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The output stage circuit comprises a DAC with gain setting and class AB output stage amplifier. The output is available as a differential signal between SPKR_A_N and SPKR_A_P for the left channel, as shown in Figure 10.9, and between SPKR_B_N and SPKR_B_P for the right channel.

The output stage is capable of driving a speaker directly when its impedance is at least 8Ω and an external regulator is used, but this will be at a reduced output swing.

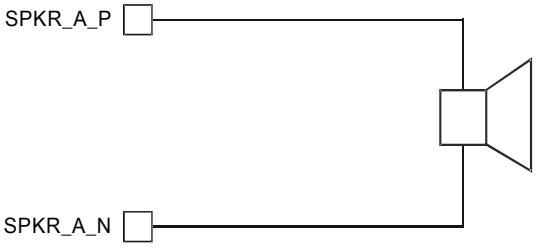


Figure 10.9: Speaker Output (Single Channel Shown)

The analogue gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

10.2.12 Mono Operation

Mono operation is a single-channel operation of the stereo CODEC. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is auxilliary mono channel that may be used in dual mono channel operation.

With single mono, the power consumption can be reduced by disabling the other channel.

10.2.13 Side Tone

In some applications it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BlueCore5-Multimedia External codec contains side tone circuitry to do this. The side tone hardware is configured through the the following PS Keys:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

10.2.14 Integrated Digital Filter

BlueCore5-Multimedia External has a programmable digital filter integrated into the ADC channel of the codec. The filter is a two stage, second order IIR and can be used for functions such as custom wind noise rejection. The filter also has optional DC blocking.

The filter has 10 configuration words used as follows:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format XX.XXXXXXXXXX

Note:

The position of the binary point is between bit 10 and bit 9, where bit 11 is the most significant bit.

For example:

01.1111111111 = most positive number, close to +2

01.0000000000 = 1

00.0000000000 = 0

11.0000000000 = -1

10.0000000000 = -2, most negative number

The equation for the IIR filter is shown in Equation 10.1. When the DC blocking is enabled the equation is shown in Equation 10.2.

The filter can be configured, enabled and disabled from the VM via the `CodecSetIIRFilterA` and `CodecSetIIRFilterB` traps[1]. The configuration function takes 10 variables in the order shown below:

`0` : Gain

`1` : b_{01}

`2` : b_{02}

`3` : a_{01}

`4` : a_{02}

`5` : b_{11}

`6` : b_{12}

`7` : a_{11}

`8` : a_{12}

`9` : DC Block (1 = enable, 0 = disable)

$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01}\, z^{-1} + b_{02}\, z^{-2})}{(1 + a_{01}\, z^{-1} + a_{02}\, z^{-2})} \times \frac{(1 + b_{11}\, z^{-1} + b_{12}\, z^{-2})}{(1 + a_{11}\, z^{-1} + a_{12}\, z^{-2})}$$

Equation 10.1: IIR Filter Transfer Function, H(z)

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 10.2: IIR Filter plus DC Blocking Transfer Function, $H_{DC}(z)$

10.3 PCM Interface

The audio *pulse code modulation* (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

PCM is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore5-Multimedia External has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. BlueCore5-Multimedia External offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore5-Multimedia External allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore5-Multimedia External can operate as the PCM interface master generating PCM_SYNC and PCM_CLK or as a PCM interface slave accepting externally generated PCM_SYNC and PCM_CLK.
BlueCore5-Multimedia External is compatible with various clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats, and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

[1] Requires firmware support

10.3.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore5-Multimedia External generates PCM_CLK and PCM_SYNC.

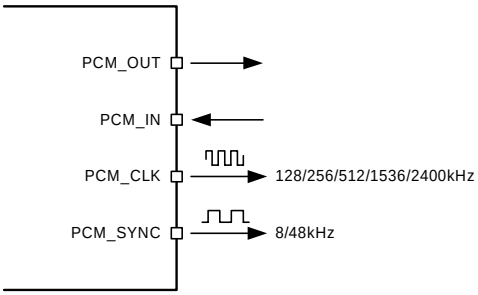


Figure 10.10: PCM Interface Master

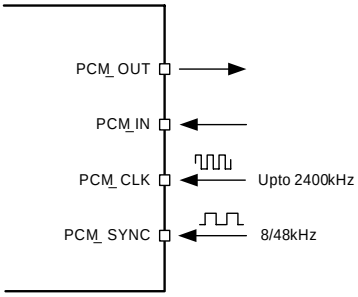


Figure 10.11: PCM Interface Slave

10.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore5-Multimedia External is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore5-Multimedia External is configured as PCM Slave, PCM_SYNC may be from one cycle PCM_CLK to half the PCM_SYNC rate.

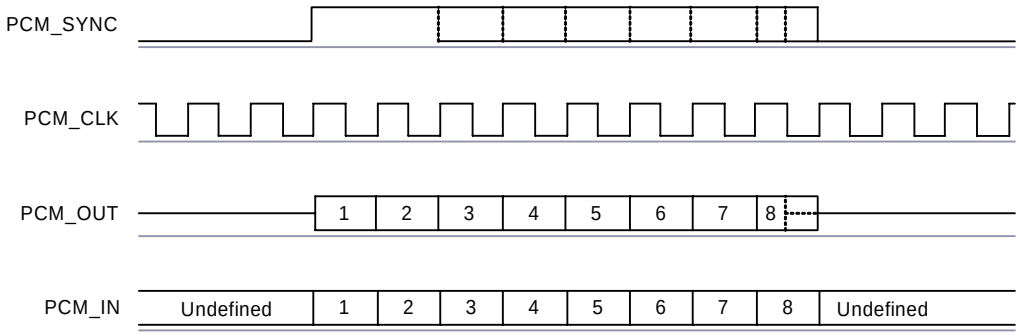


Figure 10.12: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore5-Multimedia External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

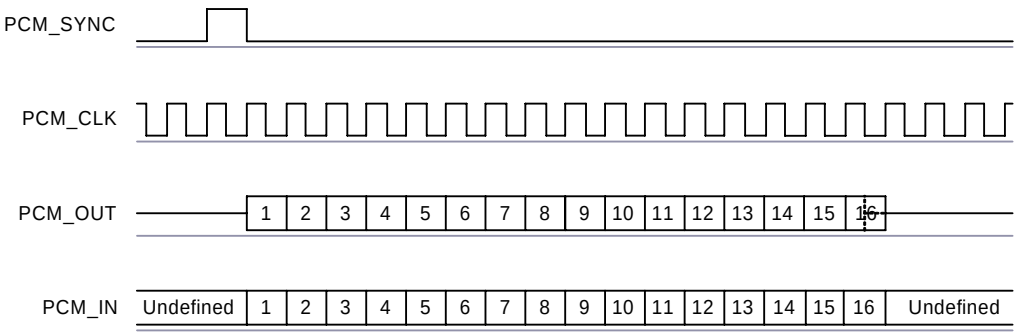


Figure 10.13: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore5-Multimedia External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.3.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

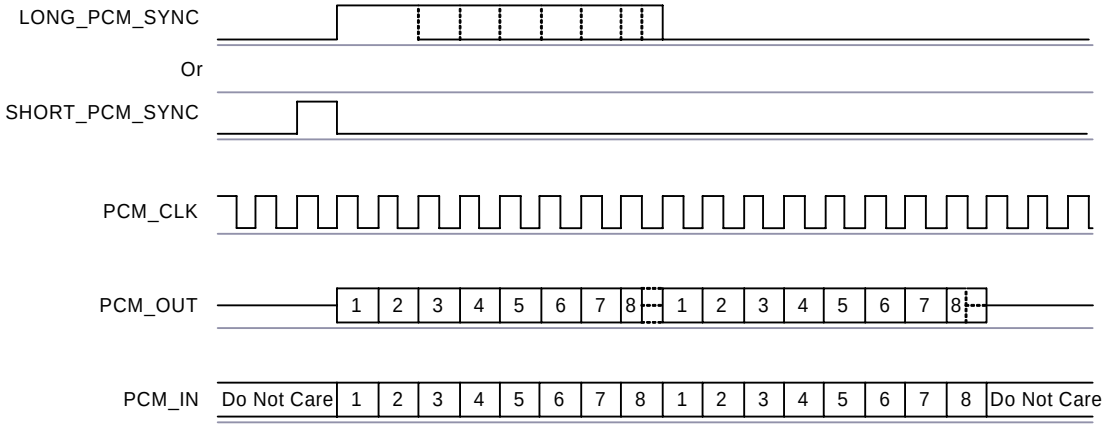


Figure 10.14: Multi-slot Operation with Two Slots and 8-bit Companded Samples

10.3.5 GCI Interface

BlueCore5-Multimedia External is compatible with the *General Circuit Interface* (GCI), a standard synchronous 2B +D ISDN timing interface. The two 64kbps B channels can be accessed when this mode is configured.

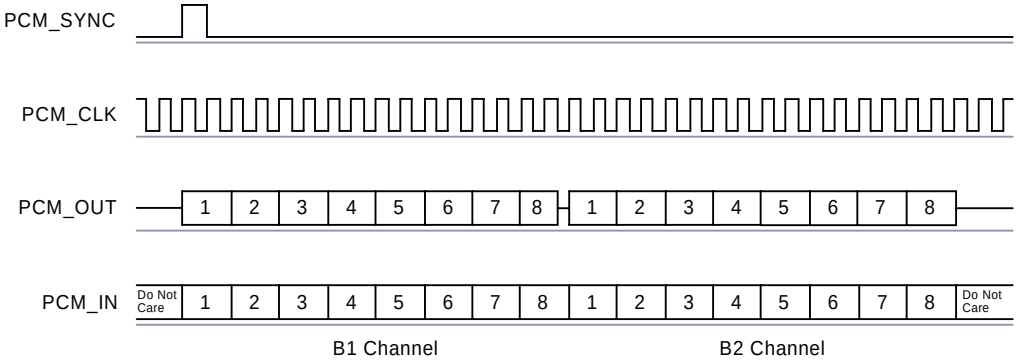


Figure 10.15: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz.

10.3.6 Slots and Sample Formats

BlueCore5-Multimedia External can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore5-Multimedia External supports 13-bit linear, 16-bit linear and 8-bit µ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

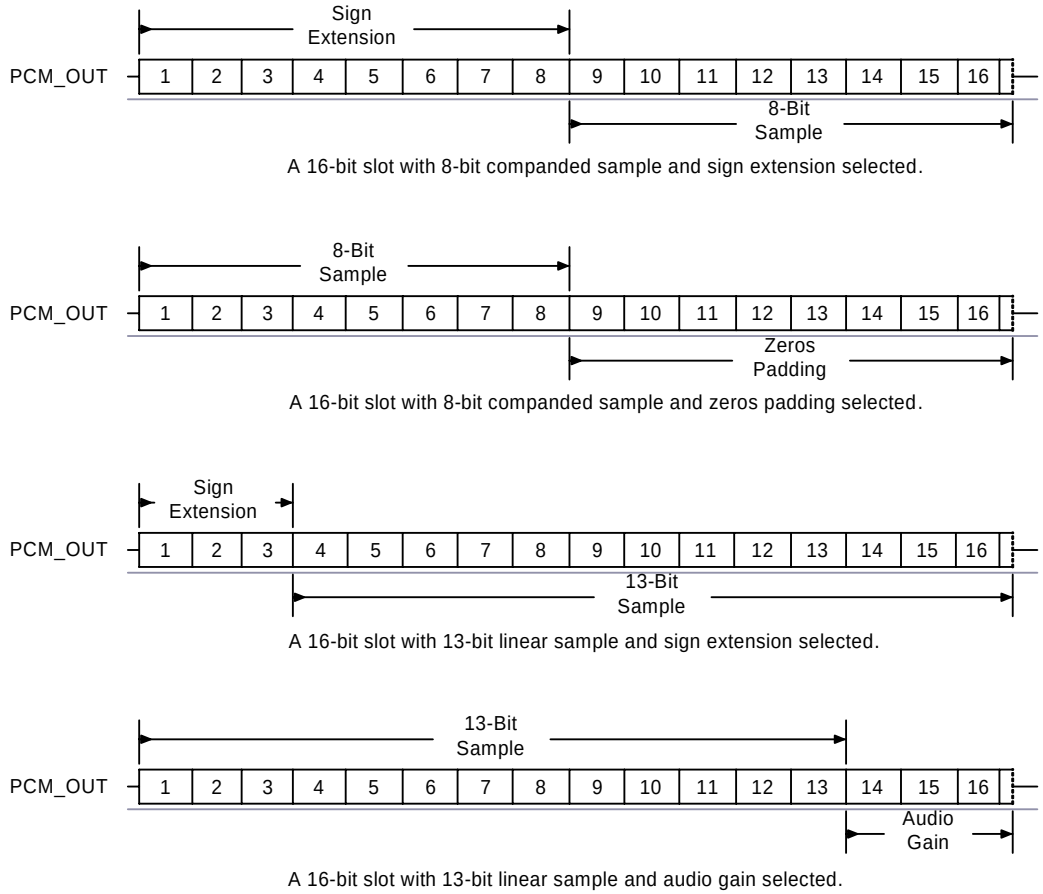


Figure 10.16: 16-Bit Slot Length and Sample Formats

10.3.7 Additional Features

BlueCore5-Multimedia External has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

10.3.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 10.10.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Selection of frequency is programmable. See Table 10.9 and Section 10.3.9.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} [(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [(a)]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 10.7: PCM Master Timing

[(a)] Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

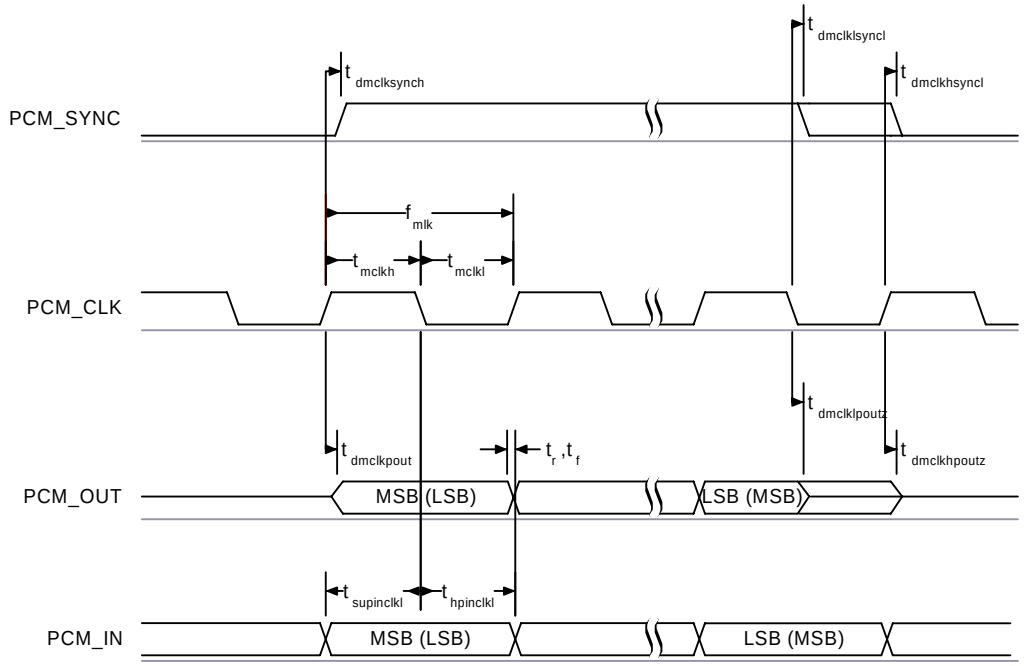


Figure 10.17: PCM Master Timing Long Frame Sync

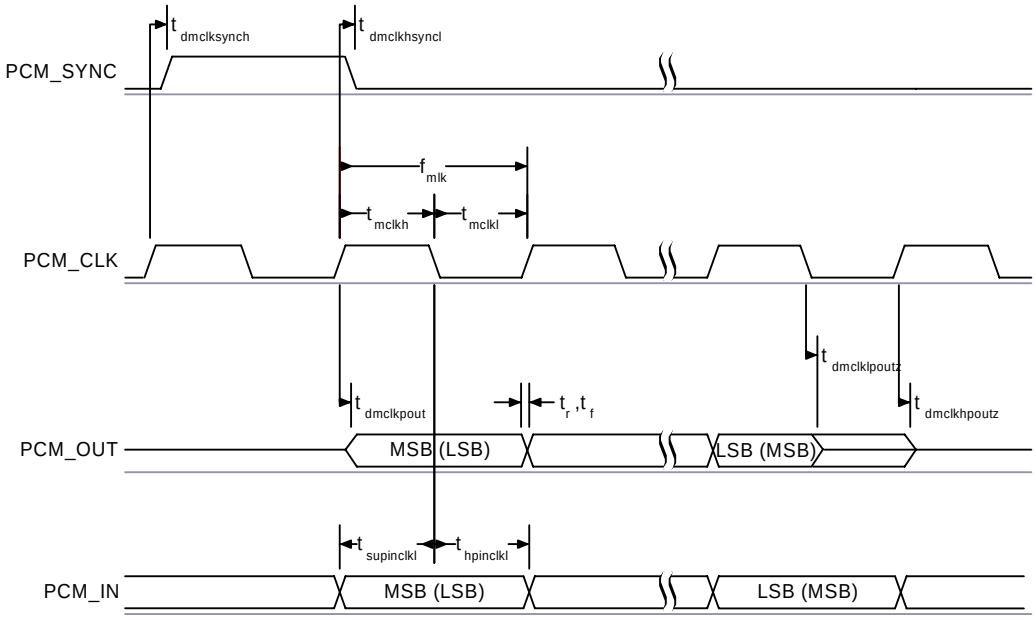


Figure 10.18: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	(a)	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	(b)	kHz
t_{sclkl}	PCM_CLK low time	80	-	-	ns
t_{sclkh}	PCM_CLK high time	80	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	20	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	20	-	-	ns

Table 10.8: PCM Slave Timing

(a) Max frequency is the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

(b) Max frequency is twice the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

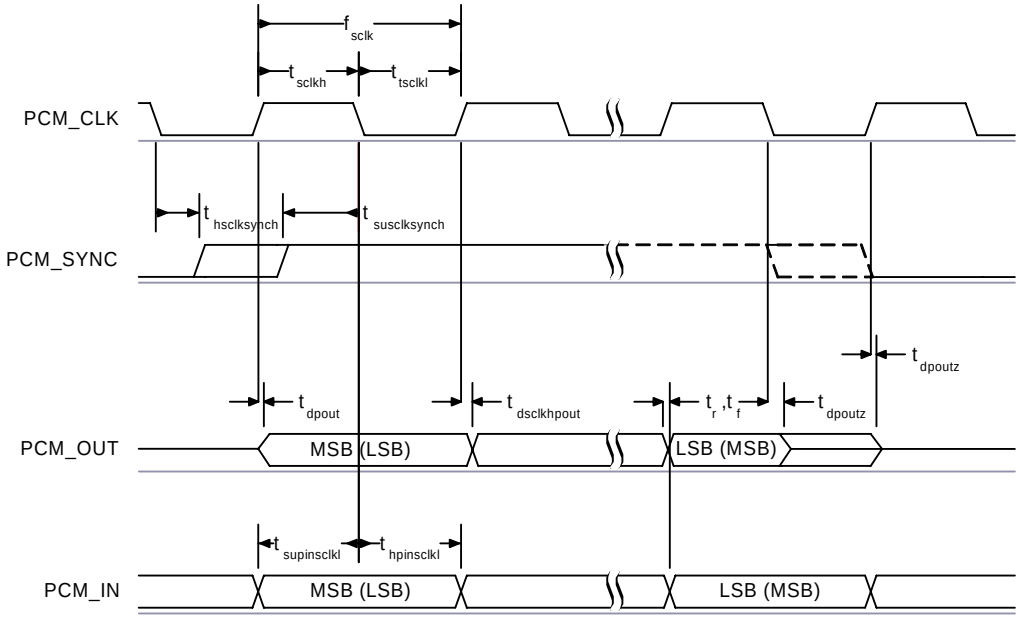


Figure 10.19: PCM Slave Timing Long Frame Sync

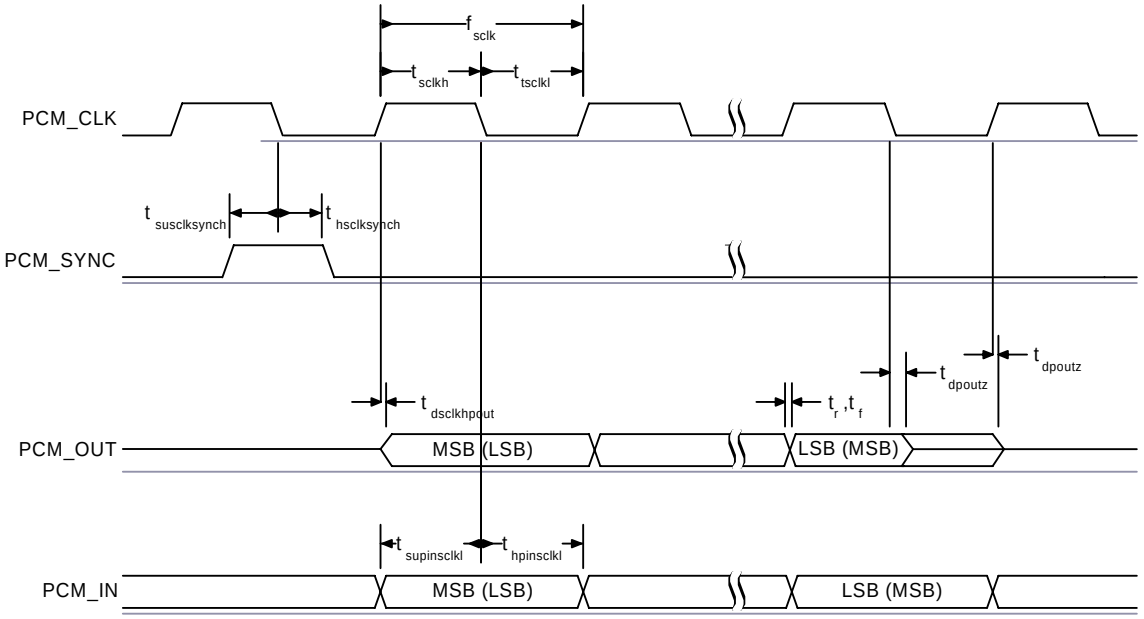


Figure 10.20: PCM Slave Timing Short Frame Sync

10.3.9 PCM_CLK and PCM_SYNC Generation

BlueCore5-Multimedia External has two methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by *Direct Digital Synthesis* (DDS) from BlueCore5-Multimedia External internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 10.3 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 10.3: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 10.4:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 10.4: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

10.3.10 PCM Configuration

The PCM configuration is set using the PS Keys, PSKEY_PCM_CONFIG32 described in Table 10.10 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 10.9. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 10.9: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.

Name	Bit Position	Description
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some CODECS use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to `0b00000`.
MASTER_CLK_RATE	[22:21]	Selects 128 (`0b01`), 256 (`0b00`), 512 (`0b10`) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (`0b00`), 16 (`0b01`), 8 (`0b10`) bit sample with 16-cycle slot duration or 8 (`0b11`) bit sample with 8-cycle slot duration.

Table 10.10: PSKEY_PCM_CONFIG32 Description

10.4 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, *left-justified* (LJ) or *right-justified* (RJ). The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 10.11 lists these alternative functions. Figure 10.21 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 10.11: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 10.12 describes the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that is used to set-up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6 dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.

Table 10.12: PSKEY_DIGITAL_AUDIO_CONFIG

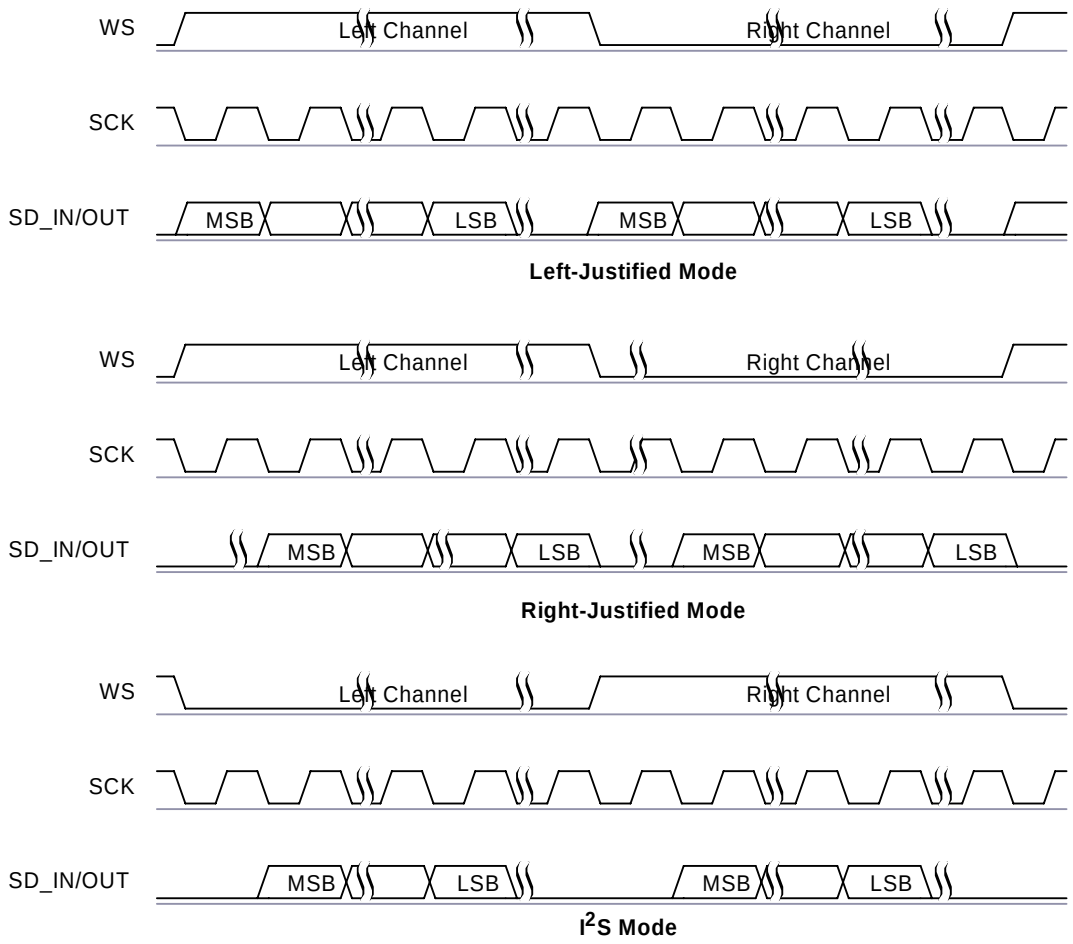


Figure 10.21: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore5-Multimedia External is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	30	ns
t_{ssu}	WS to SCK set-up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	20	-	-	ns

Table 10.13: Digital Audio Interface Slave Timing

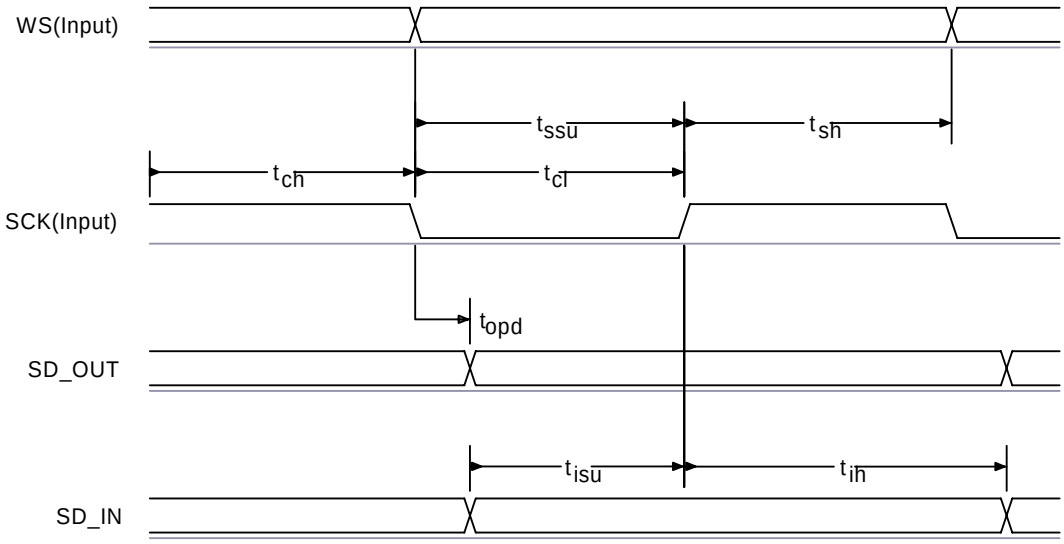


Figure 10.22: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	30	ns
t_{spd}	SCK to WS delay	-	-	30	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

Table 10.14: Digital Audio Interface Master Timing

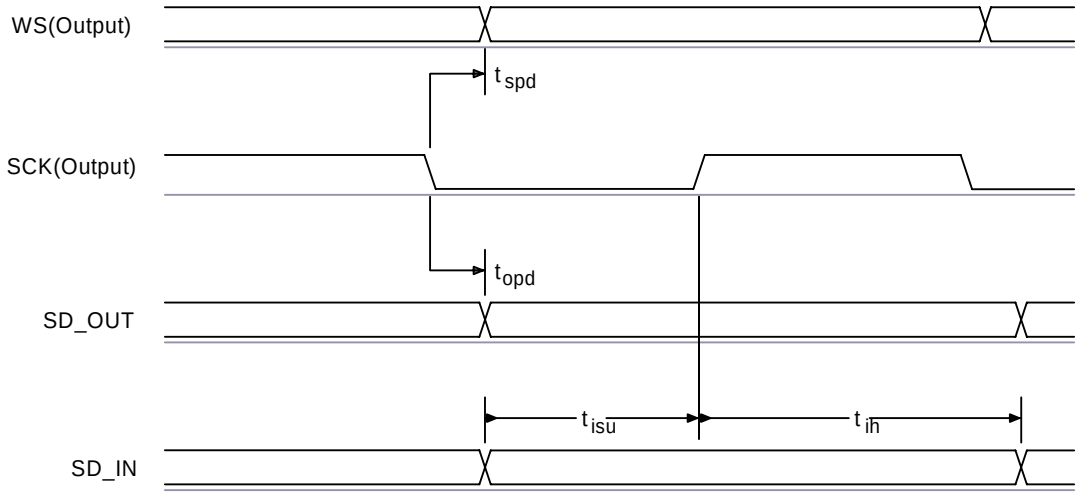


Figure 10.23: Digital Audio Interface Master Timing